IndustryPack™†Clock Generator

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This note describes an IndustryPack-base clock generator module. Output from the generator conforms to the Fermilab TCLK protocol that carries eight-bit events encoded on a 10 MHz signal. Events may be placed on the clock from events detected on an incoming clock, from external pulse inputs, and from data written to the generator by the local computer. The generator includes provision for backup in case the incoming clock disappears.

Physically, the IndustryPack Module is a 1.8" by 3.9" circuit board that contains two high density 50-pin "D" female connectors as defined by the GreenSpring IndustryPack specification. This specification is a public domain definition of a small mezzanine board for use in microprocessor-based systems. Figure 1 is a diagram of the IPClkGen module showing the parts placement including the two 50-pin connectors, one logic interface and one for user I/O signals. The logic interface includes:

D0-D15	16 bit data
IOSEL/	I/O Addr space select
INTSEL/	Interrupt Select
INTREQ0	Interrupt request
ACK/	Acknowledge control
Addr 1..6	I/O space Address lines
Reset/	Clears all registers, inhibits triggers (low active)

I/O for the clock generator board includes a TClk receiver, choice of an onboard 10 MHz oscillator for backup, an input for 15 Hz (or 10 Hz) backup, input buffers for the pulsed event input trigger signals, and output drivers for the encoded clock, the 10 MHz clock, and status bits to indicate when the 15 or 10 Hz and the 10 MHz from the input clock are no longer present.

At the present time, the Actel chip does not assert an interrupt request, but interrupt capability could be added into the Actel design if required. The Actel chip contains the following circuitry:

- IP interface logic
- TClk decoder
- Eight event input latches
- Computer event latch
- Prioritizer for eight input latches
- Prioritizer for Decoded events, input triggered events, and computer generated events
- Serializer and Manchester encoder

In operation, the clock generator used with the Tevatron clock decodes the incoming clock and passes all the events $0x, $1x, and $2x. These are the events assigned to the Fermilab Linac, Booster, and Main Ring accelerators. Pulse input events are latched separately, prioritized and output as $Ax events. A separate 4-bit latch can be written by the IP's host computer to address Base+1. A *write* to this location causes an event to be encoded onto the output serial clock. These events are output as $4x events. The reason to restrict the range of computer generated events is to avoid the inadvertent writing of preassigned events generated in hardware. Sources of events are prioritized as Decoded events, trigger input events, and computer events in that order. The order is chosen to allow a close packed group of decoded events to be output without interference from other events that are separately latched and can wait for the decoded events to be output. The computer events are given the lowest priority because they would typically be settings to the local station that arrived as a network message and have less precise timing than a pulse input trigger.

In some installations, it may be required to add events to the clock at more than one location. A jumper on the IP module can allow all decoded incoming events to be passed through and reinstalled on the output clock. Another jumper selects either the onboard 10 MHz oscillator or an offboard source as the backup clock frequency.

In the Actel chip a byte-wide register located at address Base+3 may be loaded with any clock event value. When this event is decoded from the input TClk, it will be placed on the serial clock as event $A0. The Fermilab version of the Actel chip detects all Booster reset events and them as event $A7. There are then only six active pulse input events.

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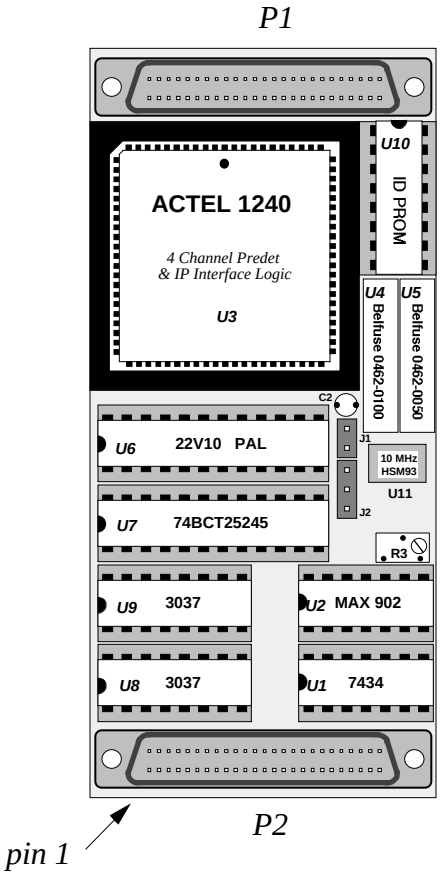
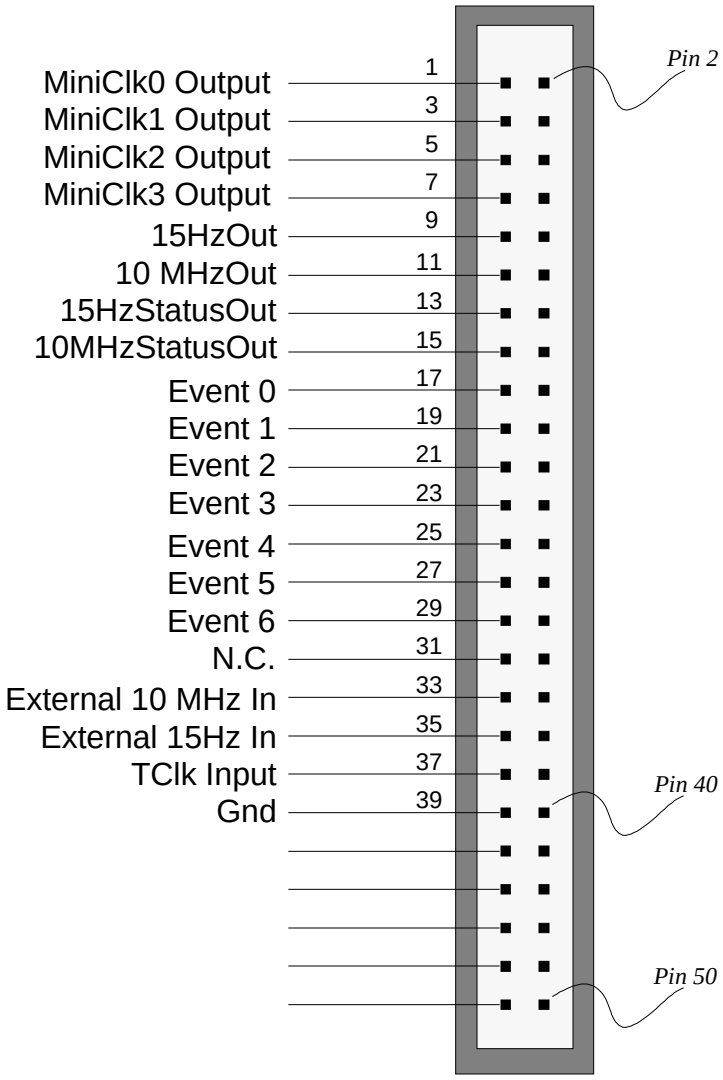
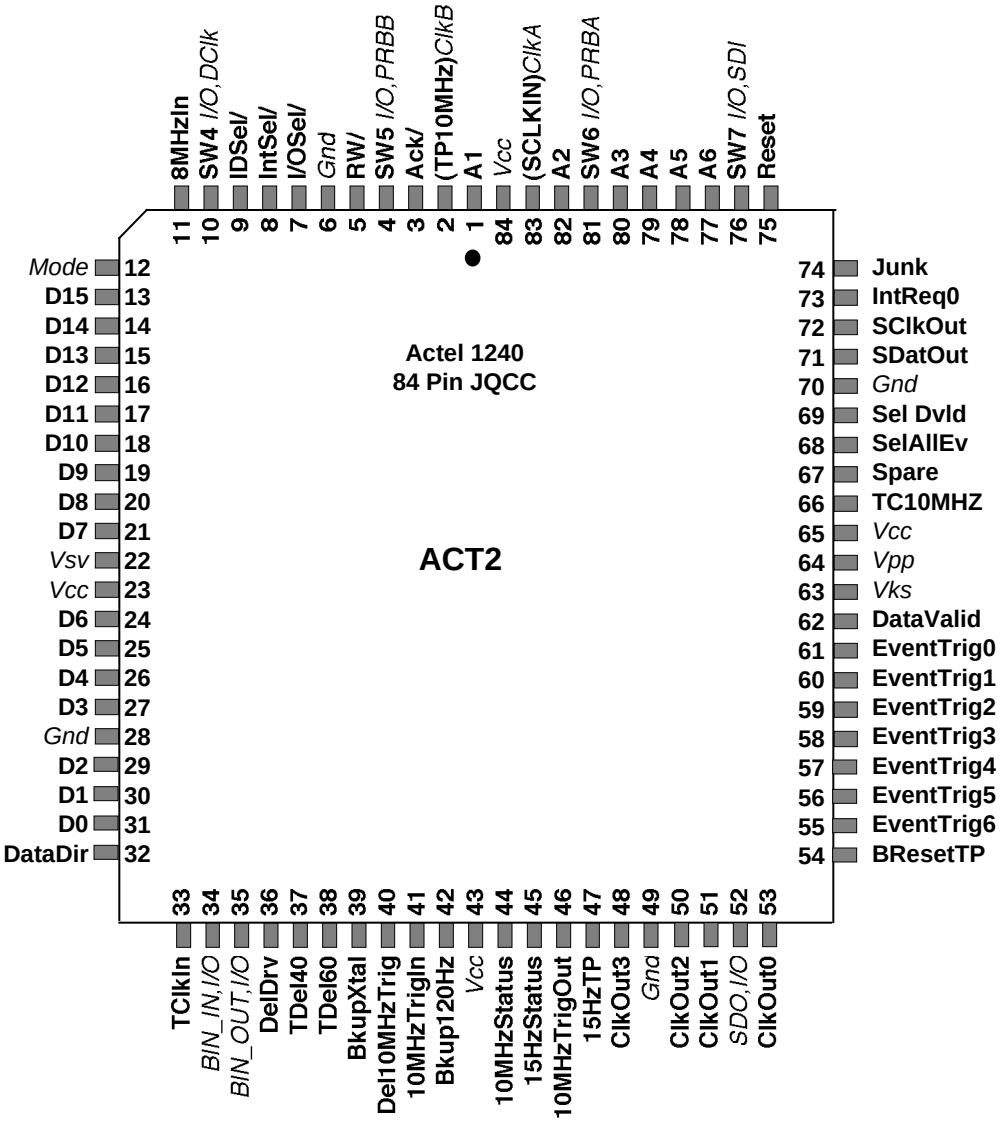


Industry Pack–Based Clock Generator Module



Notes: All Even Numbered Pins are Gnd.
Pin numbers of the IP module connector P2 are the same as for Carrier Board connector

IP MiniClk I/O Connector Pinout



ACT2 IP Clock Generator Pinout

mf. 122292